REMARKS

Claims 1-3 and 5-10 were canceled from the Parent Application for further prosecution in the present application, to facilitate allowed claims in the Parent Application to pass to issuance. Claims 1-3 and 5-10 are pending. Claims 1 and 5 are amended from the originally filed claims to their respective conditions at the time they were canceled from the Parent Application.

In the Parent Application, in response to the arguments submitted by Applicants on August 6, 2001, the Examiner states in the Advisory Action of August 29, 2001:

> Applicant's main argument includes that the prior art reference of Kim does not teach or suggest the claimed invention because the substrate (1) in Kim is not electrically floating, as Kim teaches such a structure that requires grounding of the substrate (1). In response, it is noted that no support is found in Kim for Applicant's assertion that the structure of Kim necessarily requires grounding of the substrate region (1). In fact, Kim teaches to ground the Vdd terminal connected to an emitter region (3b) which forms a vertical pnp transistor (Tr. 2) with the region (2b) as the base and the substrate region (1) as the collector (See col. 3, lines 44-50). Kim further teaches that the vertical transistor (Tr. 2) turns on when a high negative voltage is applied to the terminal of PAD (col. 4, lines 6-15). Accordingly, one of ordinary skilled in the art would readily recognize that the substrate region (1) of Kim can not be grounded when the Vdd is grounded; otherwise the emitter and the collector would be both grounded, resulting in the vertical transistor (Tr. 2) not being able to turn on.

Applicants respectfully disagree with the Examiner. Contrary to the Examiner's assertion above, the portion of Kim's disclosure upon which the Examiner relied (i.e., Col. 3, lines 44-50) does not teach grounding of the V_{dd} terminal:

> Those skilled in the art will appreciate that a pair of vertical pnp transistors Tr. 1 and Tr.2 are thus provided with respective regions 3a and 3b serving as emitters, regions 2a and 2b serving as bases, and the substrate 1 serving as a collector for each. In addition, a horizontal npn transistor Tr.3 is formed

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Version with markings to show changes made

In the Specification

On page 1, insert at line 7, before the "BACKGROUND OF THE INVENTION" section:

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CROSS-REFERENCE TO RELATED PATENT APPLICATIONS

This application is a continuation application of U.S. patent application, serial no. 09/100,384, entitled "A Dual-Direction Over-Voltage And Over-current IC Protection Device and Its Cell Structure," by Wang et al., assigned to Advanced Micro Devices, Inc., which is also the Assignee of the present application.

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In the Claims

Please amend Claims 1 and 5 as follows:

1. (Amended) An electrostatic discharge (ESD) protection structure for protecting an Integrated Circuit comprising:

a first semiconductor region of a first conductivity type;

a second semiconductor region of a second conductivity type [adjacent] in contact with said first semiconductor region;

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an electrically floating [a] third semiconductor region of [a] said first conductivity type in contact with [adjacent] said second semiconductor region and separated from said first semiconductor region by said second semiconductor region;

a fourth semiconductor region of [a] said second conductivity type [adjacent] in contact with said third semiconductor region and separated from said second semiconductor region by said third semiconductor region; and

a fifth semiconductor region of [a] said first conductivity type in contact with [adjacent] said [second] fourth semiconductor region and separated from said third semiconductor region by said fourth semiconductor region; wherein a first terminal, A, of said ESD structure is connected to said first semiconductor region and said second semiconductor region and a second terminal, K, of said ESD structure is connected to said fourth semiconductor region and said fifth semiconductor region.

5. The ESD structure of Claim [4] 1 wherein said third semiconductor region includes an n-well region formed in a p-type semiconductor substrate.

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